Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:
a plurality of unit cells connected in parallel, the unit cells each having a gate finger, wherein a pitch between the gate fingers is varied in a predetermined pattern between the gate fingers so as to provide a non-uniform pitch between the gate fingers,

wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a ~~lower peak~~ substantially uniform junction temperature to a substantial majority of the gate fingers during RF operation ~~than a corresponding uniform gate pitch device for a particular set of operating conditions~~.

2. Canceled.

3. Canceled.

4. (Original) The semiconductor device of Claim 1, wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a substantially uniform junction temperature to all but the outermost gate fingers of the device when in operation.

5. (Original) The semiconductor device of Claim 1, wherein the unit cells comprise a plurality of unit cells arranged in a linear array.

6. (Original) The semiconductor device of Claim 1, wherein the unit cells comprise a plurality of unit cells arrange in a two dimensional array and wherein the non-uniform pitch gate fingers are provided in at least one of the two dimensions of the two dimensional array.

7. (Original) The semiconductor device of Claim 6, wherein the non-uniform pitch gate fingers are provided in both dimensions of the two dimensions of the two dimensional array.

8. ((Previously presented) The semiconductor device of Claim 1, wherein the pitch between the gate fingers varies in a substantially linear pattern from a small pitch to a larger pitch toward the center of the device.

9. Canceled.

10. (Original) The semiconductor device of Claim 1, wherein the unit cells comprise MESFET unit cells.

11. (Original) The semiconductor device of Claim 1, wherein the unit cells comprise silicon carbide semiconductor device unit cells or gallium nitride semiconductor device unit cells.

12. (Original) The semiconductor device of Claim 1, wherein the predetermined pattern of non-uniform pitch between the gate fingers provides a more uniform junction temperature than a corresponding uniform gate pitch device for a particular set of operating conditions.

13. (Original) The semiconductor device of Claim 2, wherein the junction temperature does not differ by more than about 5 °C over at least 80% of the plurality of unit cells.

14. (Original) The semiconductor device of Claim 2, wherein the junction temperature does not differ by more than about 5 °C over at least 95% of the plurality of unit cells.

15. (Currently amended) A field effect transistor, comprising:

a plurality of unit cells electrically connected in parallel, each unit cell having a source region and a drain region; and

a plurality of gates of the unit cells, the plurality of gates being electrically connected in parallel and having a non-uniform spacing between the gates, wherein the non-uniform spacing between the gates is provided in a pattern that provides a lower peak junction temperature during RF operation than a corresponding uniform gate pitch device for a particular set of operating conditions.

16. (Original) The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a linear array of unit cells.

17. (Original) The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a two dimensional array of unit cells.

18. (Original) The field effect transistor of Claim 17, wherein the non-uniform spacing of the gates is in a single dimension of the two dimensional array.

19. (Original) The field effect transistor of Claim 17, wherein the non-uniform spacing of the gates is in both dimensions of the two dimensional array.

20. (Original) The field effect transistor of Claim 15, wherein the plurality of unit cells comprise a plurality of silicon carbide unit cells.

21-27. Canceled.

28. (Previously presented) The field effect transistor of Claim 15, wherein the spacing between the gates is at least 60 μm, and wherein the field effect transistor is capable of producing at least 30 W of RF output power.

28. (Previously presented) The field effect transistor of Claim 15, wherein the spacing between the gates is at least 40 μm, and wherein the field effect transistor is capable of producing at least 60 W of RF output power.

29. (Previously presented) The field effect transistor of Claim 15, wherein the spacing between the gates varies in a substantially linear pattern from a small pitch to a larger pitch toward the center of the device.